UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,675	11/21/2003	Chang Su Kyeong	049128-5125	9069

9629 7590 12/21/2006

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
SHAPIRO, LEONID	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,675	KYEONG ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9,11,13-14,16* is/are rejected.

7)☒ Claim(s) *5,6,10,12,15 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,097,362) in view of Lee (US 7,095,393).

As to claim 1, Kim teaches a driving apparatus of a liquid crystal display device (col. 1, lines 10-13), comprising:

a multiplexer array for performing time-division on inputted pixel data to supply time-divided pixel data (fig. 2, item 37, col. 3, lines 40-57);

a digital-to-analog converter array for converting the time-divided pixel data into pixel voltage signals (fig. 2, item 39, col. 3, lines 40-57); and

a demultiplexer array for driving data lines in a time-division manner to supply the converted pixel voltage signals (fig. 2, item 41, col. 3, lines 40-57),

wherein the digital-to-analog converter array receives a plurality of pixel voltage signal levels inputted from an external source and generates the pixel voltage signals using the pixel voltage signal level (fig. 2, items 37,39,41, from col. 2, line 61 to col.4,line 17).

Kim does not disclose voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data.

Lee teaches voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data (fig.7, item 400,col. 8, lines 52-63 and col. 12. lines 1-31).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Lee into Kim system in order to enhance the response speed (col. 2, lines 25-26 in the Lee reference).

As to claim 2, Kim teaches

a shift register array for sequentially generating a sampling signal (fig. 2,item 31); a latch array for sequentially latching the pixel data by designated units in response to the sampling signal to simultaneously output the latched pixel data to the first multiplexer array (fig. 2,item 33, col. 3, lines 41-57); and a buffer array for buffering the pixel voltage signal to supply the buffered signal to the demultiplexer array (fig. 2,item 45).

As to claim 3, Kim teaches the first multiplexer array includes at least an N-number (N is a positive integer) of multiplexers and performs time-division on a plurality of input pixel data to supply the time-divided pixel data, the digital-to-analog converter array converts the time-divided pixel data into the pixel voltage signals, and the demultiplexer array includes at least an N-number of demultiplexers and supplies the

pixel voltage signals to a plurality of data lines (fig. 2, items 37,39,41, from col. 2, line 40 to col.4,line 17).

As to claim 13, Kim teaches a driving apparatus of a liquid crystal display device (col. 1, lines 10-13), comprising:

performing time-division on pixel data inputted from an external source to output time-divided pixel data (fig. 2, item 37, col. 3, lines 40-57);

converting the time-divided pixel data into pixel voltage signals (fig. 2, item 39, col. 3, lines 40-57); and

performing time-division manner on data lines to supply the converted pixel voltage signals (fig. 2, item 41, col. 3, lines 40-57),

performing time-division on pixel data inputted from an external source to output time-divided pixel data (fig. 2, items 37,39,41, from col. 2, line 61 to col.4,line 17).

Kim does not disclose voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data.

Lee teaches voltage signals using the pixel voltage signal level with a voltage at least one-step higher in absolute value than the original pixel voltage signal level in correspondence to at least one pixel data (fig.7,item 400,col. 8, lines 52-63 and col. 12. lines 1-31).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Lee into Kim system in order to enhance the response speed (col. 2, lines 25-26 in the Lee reference).

3. Claims 4,7-9,11,14,16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim and Lee as applied to claim 3 above, and further in view of Jeong (US 6,335,721 B1).

As to claim 4, Kim and Lee do not disclose at least an "N+l"-number of positive and negative digital-to-analog converters for converting the time-divided pixel data into the pixel voltage signals, wherein the positive and negative digital-to-analog converters are alternately arranged.

Jeong teaches "N "-number of positive and negative digital-to-analog converters for converting the time-divided pixel data into the pixel voltage signals, wherein the positive and negative digital-to-analog converters are alternately arranged (Fig. 4, item 500, col. 6, lines 21-30).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Jeong into Lee and Kim system in order to reduce number of components (col. 2, lines 51-52 in the Jeong reference).

As to claims 7-8, Jeong teaches the N-number of the first multiplexers include an odd-numbered multiplexer performs time- division on odd-numbered pixel data in response to an inputted first selection control signal to output the time-divided data, and an even-numbered multiplexer performs time- division on even-numbered pixel data in

response to an inputted second selection control signal to output the time-divided data (figs. 4-5,items 100,300, col. 4, lines 27-60 and col. 5., lines 60-67).

As to claims 9,11 Jeong teaches the first and second selection control signals have a logical state opposite to each other, and the logical state is inverted at least for each half or quarter horizontal period (col. 1, lines 42-46).

As to claims 14,16 Kim and Lee do not disclose one horizontal period is divided into two half horizontal periods and the pixel data are time-divided to be supplied.

Jeong teaches one horizontal period is divided into multiple horizontal periods and the pixel data are time-divided to be supplied (fig.6, col. 5, lines19-59).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate teachings of Jeong into Lee and Kim system in relation to two halves of horizontal periods in order to reduce number of components (col. 2, lines 51-52 in the Jeong reference).

Allowable Subject Matter

4. Claims 5-6,10,12,15,17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claim 5 the major difference between the teaching of the prior art of record (Kim and Lee) and the instant invention is that a second multiplexer array for determining a progress path of the time-divided pixel data in response to an input polarity control signal to make the time-divided pixel data inputted to at least an N-

number of positive and negative digital-to-analog converters among at least the N-number of positive and negative digital-to-analog converters; and a third multiplexer array for determining a progress path of the pixel voltage signal in response to the polarity control signal to make the pixel voltage signal inputted to the demultiplexer array.

Claim 6 depends on claim 5.

Relative to claims 10,12 and 15,17 the major difference between the teaching of the prior art of record (Kim, Jeong and Lee) and the instant invention is that the digital-to-analog converter array generates the pixel voltage signal in use of the pixel voltage signal level having a voltage at least one step higher in absolute value than the original pixel voltage signal level in correspondence to the pixel data outputted during the first half of one horizontal period, and generates the pixel voltage signal in use of the original pixel voltage signal level in correspondence to the pixel data outputted during the second half of the one horizontal period.

Telephone Inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 571-272-7683. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LS
12.18.06

RICHARD HJERPE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600